

# FM25040A

## 4Kb FRAM Serial Memory

# RAMTRON

### Features

#### 4K bit Ferroelectric Nonvolatile RAM

- Organized as 512 x 8 bits
- High Endurance 1 Trillion ( $10^{12}$ ) Read/Writes
- 45 year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

#### Very Fast Serial Peripheral Interface - SPI

- Up to 20 MHz maximum Bus Frequency
- Direct hardware replacement for EEPROM
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)

#### Sophisticated Write Protection Scheme

- Hardware Protection
- Software Protection

#### Low Power Consumption

- 10  $\mu$ A Standby Current

#### Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 8-pin “Green”/RoHS SOIC (-G)

### Description

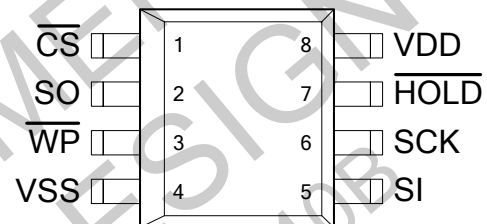
The FM25040A is a 4-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile but operates in other respects as a RAM. It provides reliable data retention for 45 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

Unlike serial EEPROMs, the FM25040A performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte has been transferred to the device. The next bus cycle may commence without the need for data polling. In addition the product offers substantial write endurance compared with other nonvolatile memories. The FM25040A is capable of supporting up to  $10^{12}$  read/write cycles, far more than most systems will require from a serial memory.

These capabilities make the FM25040A ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss.

The FM25040A provides substantial benefits to users of serial EEPROM, in a hardware drop-in replacement. The FM25040A uses the high-speed SPI bus which enhances the high-speed write capability of FRAM technology. Device specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

### Pin Configuration



Pin Names	Function
/CS	Chip Select
/WP	Write Protect
/HOLD	Hold
SCK	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
VDD	Supply Voltage 5V
VSS	Ground

Ordering Information	
FM25040A-G	“Green” 8-pin SOIC
FM25040A-GTR	“Green” 8-pin SOIC, Tape & Reel
FM25040A-S *	8-pin SOIC
FM25040A-STR *	8-pin SOIC, Tape & Reel

\* End of life. Last time buy June 2009.

This product conforms to specifications per the terms of the Ramtron standard warranty. The product has completed Ramtron’s internal qualification testing and has reached production status.

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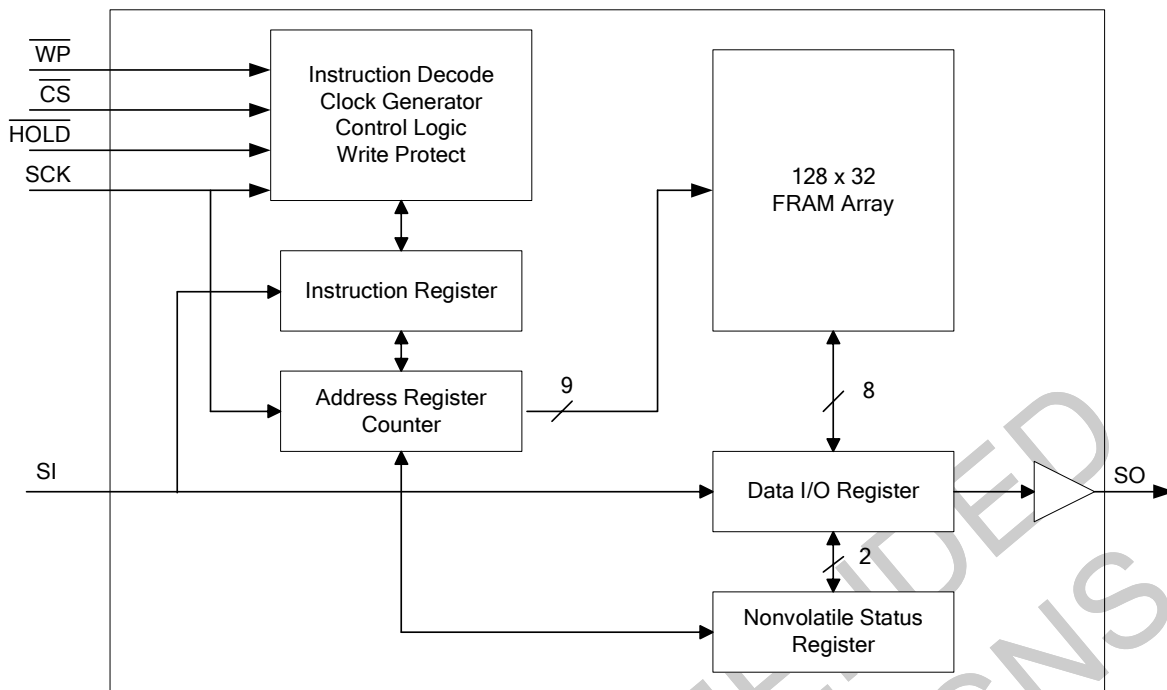


Figure 1. Block Diagram

Pin Descriptions

Pin Name	I/O	Description
/CS	Input	Chip Select. This active-low input activates the device. When high, the device enters low-power standby mode, ignores other inputs, and all outputs are tri-stated. When low, the device internally activates the SCK signal. A falling edge on /CS must occur prior to every op-code.
SCK	Input	Serial Clock: All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Since the device is static, the clock frequency may be any value between 0 and 20 MHz and may be interrupted at any time.
/HOLD	Input	Hold: The /HOLD pin is used when the host CPU must interrupt a memory operation for another task. When /HOLD is low, the current operation is suspended. The device ignores any transition on SCK or /CS. All transitions on /HOLD must occur while SCK is low.
/WP	Input	Write Protect: This active-low pin prevents all write operations, including those to the status register. If high, write access is determined by the other write protection features, as controlled through the status register. A complete explanation of write protection is provided on page 6.
SI	Input	Serial Input: All input data is driven to this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet I <sub>DD</sub> specifications. * SI may be connected to SO for a single pin data interface.
SO	Output	Serial Output: SO is the data output pin. It is driven actively during a read and remains tri-state at all other times including when /HOLD is low. Data transitions are driven on the falling edge of the serial clock. * SO can be connected to SI for a single pin data interface since the part communicates in half-duplex fashion.
VDD	Supply	Supply Voltage: 5V
VSS	Supply	Ground

## Overview

The FM25040A is a serial FRAM memory. The memory array is logically organized as 512 x 8 and is accessed using an industry standard Serial Peripheral Interface or SPI bus. Functional operation of the FRAM is similar to serial EEPROMs. The major difference between the FM25040A and a serial EEPROM with the same pin-out relates to its superior write performance. The FM25040A differs from Ramtron's FM25040 by increasing its performance to 20MHz and adding support for SPI Mode 3. This makes the FM25040A a drop-in replacement for most 4Kb SPI EEPROMs that support Modes 0 & 3.

## Memory Architecture

When accessing the FM25040A, the user addresses 512 locations each with 8 data bits. These data bits are shifted serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an op-code including the upper address bit, and a word address. The word address consists of the lower 8-address bits. The complete address of 9-bits specifies each byte address uniquely.

Most functions of the FM25040A either are controlled by the SPI interface or are handled automatically by on-board circuitry. The access time for memory operation essentially is zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. That is, by the time a new bus transaction can be shifted into the part, a write operation will be complete. This is explained in more detail in the interface section that follows.

Users expect several obvious system benefits from the FM25040A due to its fast write cycle and high endurance as compared with EEPROM. However there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since it is completed quickly. By contrast, an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

**Note that the FM25040A contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that  $V_{DD}$  is within datasheet tolerances to prevent incorrect operation. It is recommended that the part is not powered down with chip enable active.**

## Serial Peripheral Interface – SPI Bus

The FM25040A employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 20 MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25040A operates in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. A typical system configuration uses one or more FM25040A devices with a microcontroller that has a dedicated SPI port, as Figure 2 illustrates. Note that the clock, data-in, and data-out pins are common among all devices. The Chip Select and Hold pins must be driven separately for each FM25040A device.

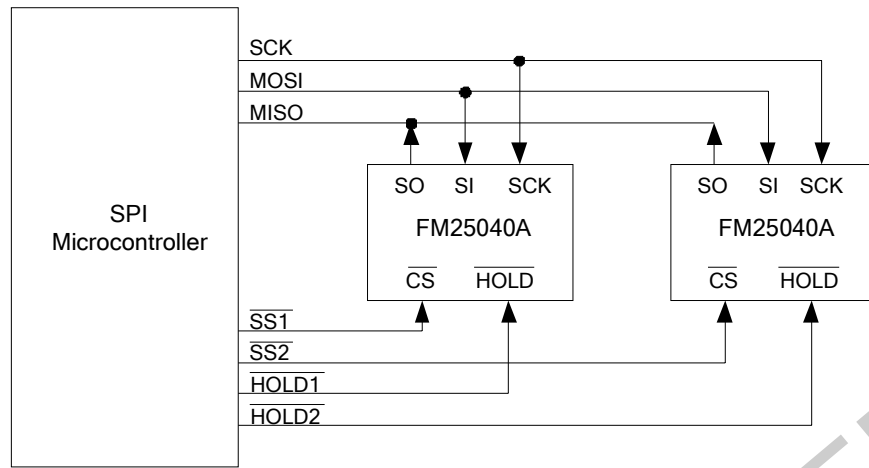
For a microcontroller that has no dedicated SPI bus, a general purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together and tie off (high) the /HOLD pin. Figure 3 shows a configuration that uses only three pins.

### Protocol Overview

The SPI interface is a synchronous serial interface using clock and data lines. It is intended to support multiple devices on the bus. Each device is activated using a chip select. Once chip select is activated by the bus master, the FM25040A will begin monitoring the clock and data lines. The relationship between the falling edge of /CS, the clock and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM25040A supports Modes 0 and 3. Figure 4 shows the required signal relationships for Modes 0 and 3. For both modes, data is clocked into the FM25040A on the rising edge of SCK and data is expected on the first rising edge after /CS goes active. If the clock begins from a high state, it will fall prior to beginning data transfer in order to create the first rising edge.

The SPI protocol is controlled by op-codes. These op-codes specify the commands to the part. After /CS is activated the first byte transferred from the bus master is the op-code. Following the op-code, any addresses and data are then transferred. Note that the WREN and WRDI op-codes are commands with no subsequent data transfer.

**Important: The /CS must go inactive (high) after an operation is complete and before a new op-code can be issued. There is one valid op-code only per active chip select.**



MOSI : Master Out Slave In  
 MISO : Master In Slave Out  
 SS : Slave Select

Figure 2. System Configuration with SPI port

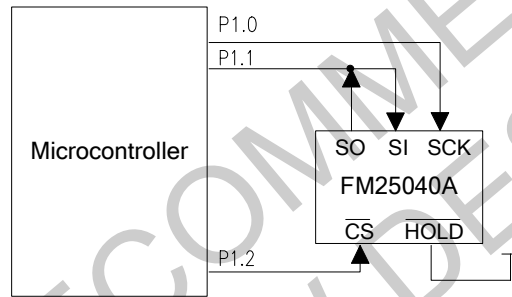
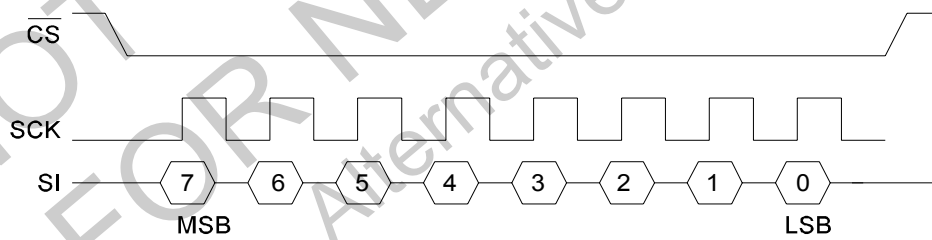


Figure 3. System Configuration without SPI port

SPI Mode 0: CPOL=0, CPHA=0



SPI Mode 3: CPOL=1, CPHA=1

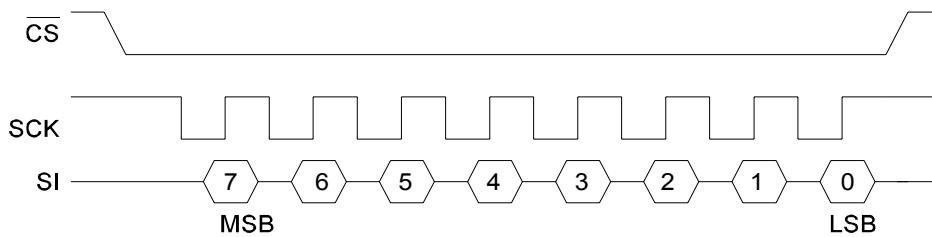


Figure 4. SPI Modes 0 & 3

**Data Transfer**

All data transfers to and from the FM25040A occur in 8-bit groups. They are synchronized to the clock signal (SCK) and they transfer most significant bit (MSB) first. The serial input data is clocked in on the rising edge of SCK. The serial data output is driven from the falling edge of SCK.

**Command Structure**

There are six commands called op-codes that can be issued by the bus master to the FM25040A. They are listed in the table below. These op-codes control the functions performed by the memory. They can be divided into three categories. First, there are commands that have no subsequent data transfer. They perform a single function, such as, enabling a write operation. Second are commands followed by one byte, either in or out. They operate on the status register. Third are commands for memory transactions followed by address and one or more bytes of data.

**Table 1. Op-code Commands**

Name	Description	Op-code
WREN	Set Write Enable Latch	0000_0110b
WRDI	Write Disable	0000_0100b
RDSR	Read Status Register	0000_0101b
WRSR	Write Status Register	0000_0001b
READ	Read Memory Data	0000_A011b
WRITE	Write Memory Data	0000_A010b

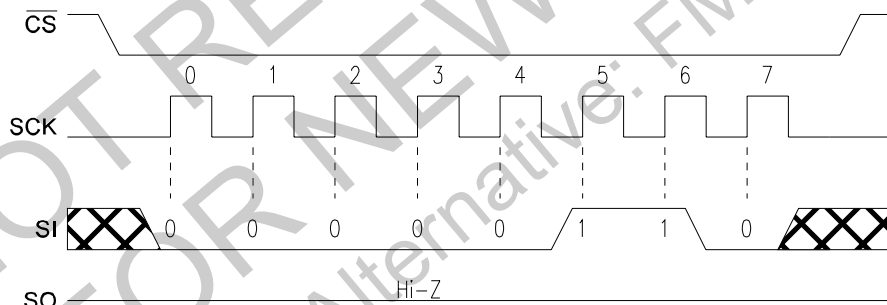
**WREN - Set Write Enable Latch**

The FM25040A will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the status register and writing the memory.

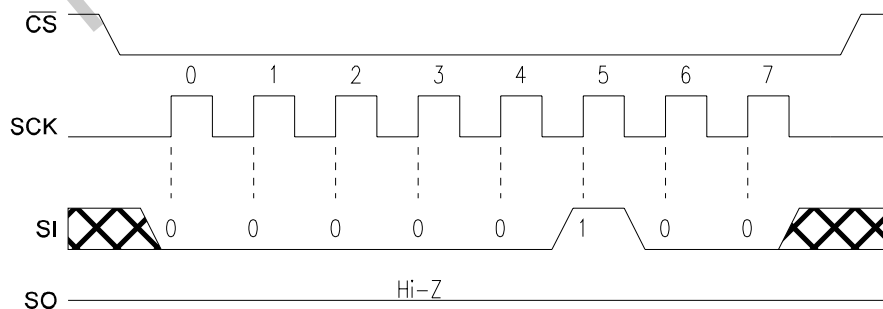
Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the status register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. A write to the status register has no effect on the WEL bit. Completing any write operation will automatically clear the write-enable latch and prevent further writes without another WREN command. Figure 5 below illustrates the WREN command bus configuration.

**WRDI - Write Disable**

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the status register and verifying that WEL=0. Figure 6 illustrates the WRDI command bus configuration.



**Figure 5. WREN Bus Configuration**



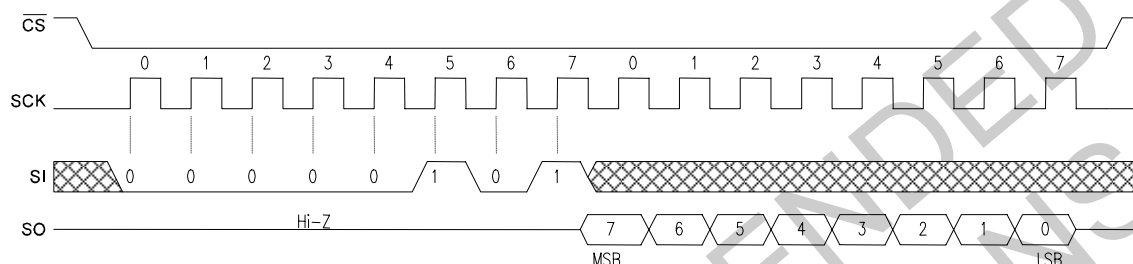
**Figure 6. WRDI Bus Configuration**

**RDSR - Read Status Register**

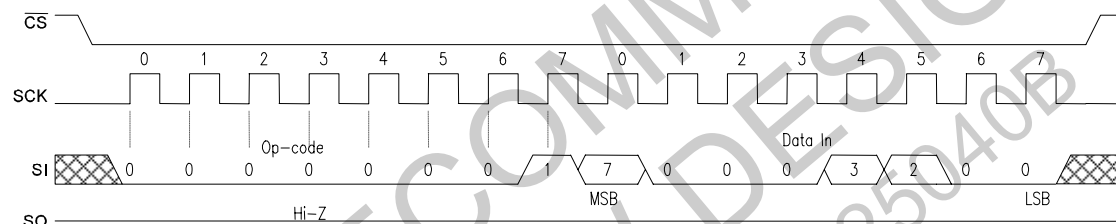
The RDSR command allows the bus master to verify the contents of the Status Register. Reading Status provides information about the current state of the write protection features. Following the RDSR op-code, the FM25040A will return one byte with the contents of the Status Register. The Status Register is described in detail in the Status Register & Write Protection section.

**WRSR – Write Status Register**

The WRSR command allows the user to select certain write protection features by writing a byte to the Status Register. Prior to issuing a WRSR command, the /WP pin must be high or inactive. Note that on the FM25040A, /WP prevents writing to the Status Register and the memory array. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch. The bus timing for RDSR and WRSR are shown below.



**Figure 7. RDSR Bus Timing**



**Figure 8. WRSR Bus Timing**

**Status Register & Write Protection**

The write protection features of the FM25040A are multi-tiered. First, a WREN op-code must be issued prior to any write operation. Assuming that writes are enabled using WREN, writes to memory are controlled by the /WP pin and the Status Register. When /WP is low, the entire part is write-protected. When /WP is high, the memory protection is subject to the Status register. Writes to the Status Register are performed using the WREN and WRSR commands and subject to the /WP pin. The Status Register is organized as follows.

**Table 2. Status Register**

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	BP1	BP0	WEL	0

Bits 0 and 4-7 are fixed at 0 and cannot be modified. Note that bit 0 (/RDY in EEPROMs) is wired low since FRAM writes have no delay and the memory is never busy. All EEPROMs use Ready to indicate

whether a write cycle is complete or not. The BP1 and BP0 bits control write protection features. They are nonvolatile (shaded yellow). The WEL flag indicates the state of the Write Enable Latch. This bit is internally set by the WREN command and is cleared by terminating a write cycle (/CS high) or by using the WRDI command.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in the following table.

**Table 3. Block Memory Write Protection**

BP1	BP0	Protected Address Range
0	0	None
0	1	180h to 1FFh (upper ¼)
1	0	100h to 1FFh (upper ½)
1	1	000h to 1FFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The BP1 and BP0 bits allow software to selectively write protect the array. These settings are only used when the /WP pin is inactive and the WREN command has been issued. The following table summarizes the write protection conditions.

**Table 4. Write Protection**

WEL	/WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	Protected	Protected	Protected
1	0	Protected	Protected	Protected
1	1	Protected	Unprotected	Unprotected

## Memory Operation

The SPI interface, with its relatively high maximum clock frequency, highlights the fast write capability of the FRAM technology. Unlike SPI-bus EEPROMs, the FM25040A can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

### Write Operation

All writes to the memory array begin with a WREN op-code. The bus master then issues a WRITE op-code. Part of this op-code includes the upper bit of the memory address. Bit 3 in the op-code corresponds to A8. The next byte is the lower 8-bits of the address A7-A0. In total, the 9-bits specify the address of the first byte of the write operation. Subsequent bytes are data and they are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 1FFh is reached, the counter will roll over to 000h. Data is written MSB first.

Unlike EEPROMs, any number of bytes can be written sequentially and each byte is written to memory immediately after it is clocked in (after the 8<sup>th</sup> clock). The rising edge of /CS terminates a WRITE op-code operation.

### Read Operation

After the falling edge of /CS, the bus master can issue a READ op-code. Part of this op-code includes the upper bit of the memory address. The next byte is the lower 8-bits of the address. In total, the 9-bits specify the address of the first byte of the read operation. After the op-code is complete, the SI pin is ignored. The bus master then issues 8 clocks, with one bit read out for each. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 1FFh is reached, the counter will roll over to 000h. Data is read MSB first. The rising edge of /CS terminates a READ op-code operation. The bus configuration for read and write operations is shown below.

### Hold

The /HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master takes the /HOLD pin low while SCK is low, the current operation will pause. Taking the /HOLD pin high while SCK is low will resume an operation. The transitions of /HOLD must occur while SCK is low, but the SCK pin can toggle during a hold state.

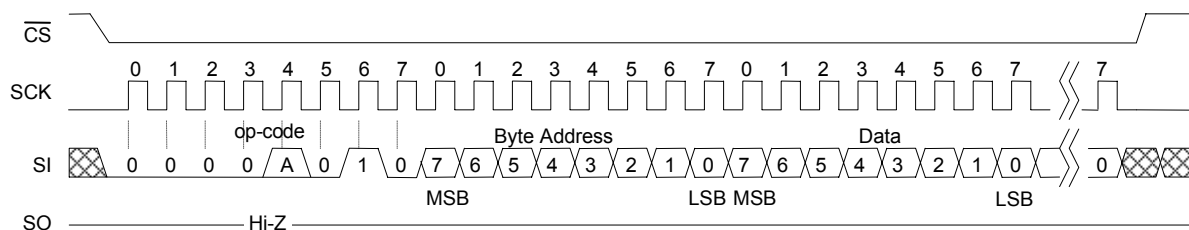


Figure 9. Memory Write

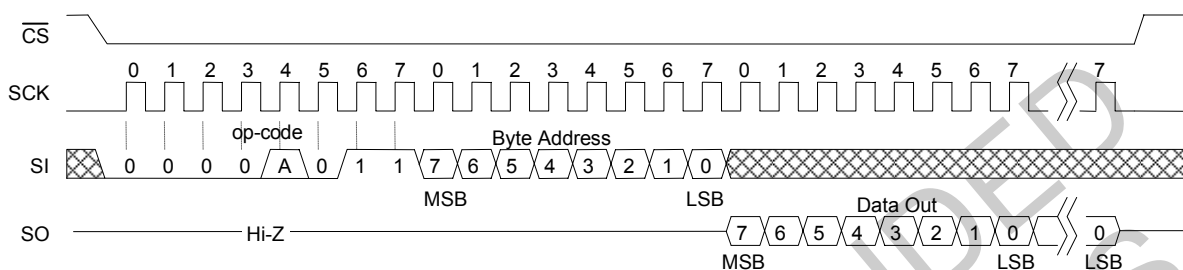


Figure 10. Memory Read

**Endurance**

Internally, a FRAM operates with a read and restore mechanism similar to a DRAM. Therefore, endurance cycles are applied for each access: read or write. The FRAM architecture is based on an array of rows and columns. Each access causes an endurance cycle for an entire row. Therefore, data locations targeted for substantially differing numbers of cycles

should not be located within the same row. In the FM25040A, there are 128 rows each 32 bits wide. Regardless, FRAM read and write endurance is effectively unlimited at the 20 MHz clock speed. Even at 2000 accesses per second to the same row, 15 years time will elapse before 10<sup>12</sup> endurance cycles occur.



## Electrical Specifications

### Absolute Maximum Ratings

Symbol	Description	Ratings
$V_{DD}$	Power Supply Voltage with respect to $V_{SS}$	-1.0V to +7.0V
$V_{IN}$	Voltage on any pin with respect to $V_{SS}$	-1.0V to +7.0V and $V_{IN} < V_{DD} + 1.0V$
$T_{STG}$	Storage Temperature	-55°C to +125°C
$T_{LEAD}$	Lead Temperature (Soldering, 10 seconds)	300°C
$V_{ESD}$	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A) - Machine Model (JEDEC Std JESD22-A115-A)	4kV 1kV 400V
	Package Moisture Sensitivity Level	MSL-1

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

### DC Operating Conditions ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{DD} = 4.5V$ to $5.5V$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{DD}$	Main Power Supply	4.5	5.0	5.5	V	
$I_{DD}$	VDD Supply Current @ SCK = 1.0 MHz @ SCK = 20.0 MHz		0.2 4	0.4 8.0	mA mA	1
$I_{SB}$	Standby Current		-	10	$\mu\text{A}$	2
$I_{LI}$	Input Leakage Current			$\pm 1$	$\mu\text{A}$	3
$I_{LO}$	Output Leakage Current			$\pm 1$	$\mu\text{A}$	3
$V_{IH}$	Input High Voltage	$0.7 V_{DD}$		$V_{DD} + 0.5$	V	
$V_{IL}$	Input Low Voltage	-0.3		$0.3 V_{DD}$	V	
$V_{OH}$	Output High Voltage @ $I_{OH} = -1\text{ mA}$	$V_{DD} - 0.8$		-	V	
$V_{OL}$	Output Low Voltage @ $I_{OL} = 2\text{ mA}$	-		0.4	V	
$V_{HYS}$	Input Hysteresis	$0.05 V_{DD}$		-	V	4

### Notes

- SCK toggling between  $V_{DD} - 0.3V$  and  $V_{SS}$ , other inputs  $V_{SS}$  or  $V_{DD} - 0.3V$ .
- SCK = SI = /CS =  $V_{DD}$ . All inputs  $V_{SS}$  or  $V_{DD}$ .
- $V_{IN}$  or  $V_{OUT} = V_{SS}$  to  $V_{DD}$ .
- This parameter is periodically sampled and not 100% tested.

**AC Parameters** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$  unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
$f_{CK}$	SCK Clock Frequency	0	20	MHz	
$t_{CH}$	Clock High Time	22		ns	1
$t_{CL}$	Clock Low Time	22		ns	1
$t_{CSU}$	Chip Select Setup	10		ns	
$t_{CSH}$	Chip Select Hold	10		ns	
$t_{OD}$	Output Disable		20	ns	2
$t_{ODV}$	Output Data Valid		20	ns	
$t_{OH}$	Output Hold	0		ns	
$t_D$	Deselect Time	60		ns	
$t_R$	Data In Rise Time		50	ns	1,3
$t_F$	Data In Fall Time		50	ns	1,3
$t_{SU}$	Data Setup Time	5		ns	
$t_H$	Data Hold Time	5		ns	
$t_{HS}$	/Hold Setup Time	10		ns	
$t_{HH}$	/Hold Hold Time	10		ns	
$t_{HZ}$	/Hold Low to Hi-Z		20	ns	2
$t_{LZ}$	/Hold High to Data Active		20	ns	2

**Notes**

- $t_{CH} + t_{CL} = 1/f_{CK}$ .
- Rise and fall times measured between 10% and 90% of waveform.
- This parameter is characterized and not 100% tested.

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f=1.0\text{ MHz}$ ,  $V_{DD} = 5\text{V}$ )

Symbol	Parameter	Max	Units	Notes
$C_O$	Output Capacitance (SO)	8	pF	1
$C_I$	Input Capacitance	6	pF	1

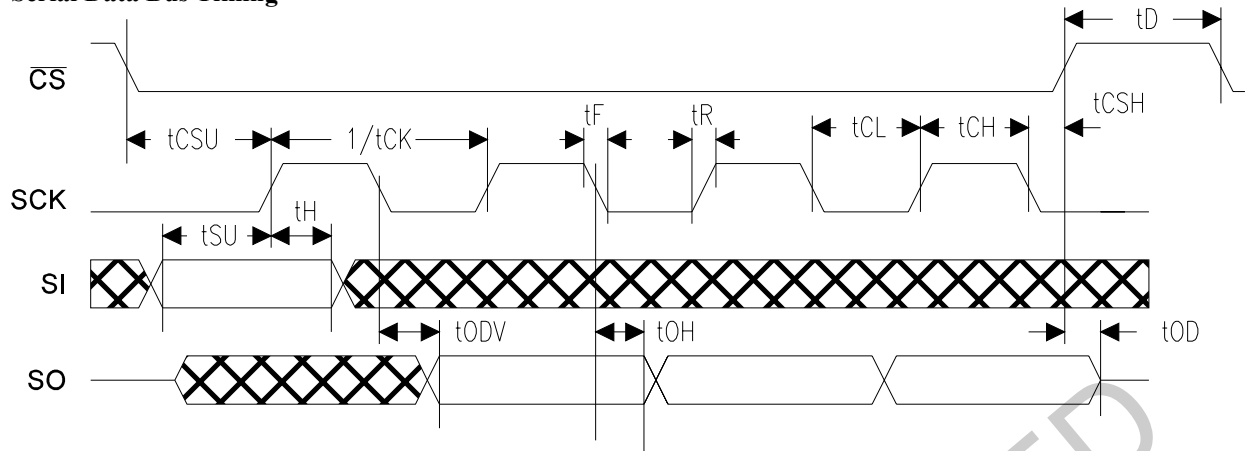
**Notes**

- This parameter is periodically sampled and not 100% tested.

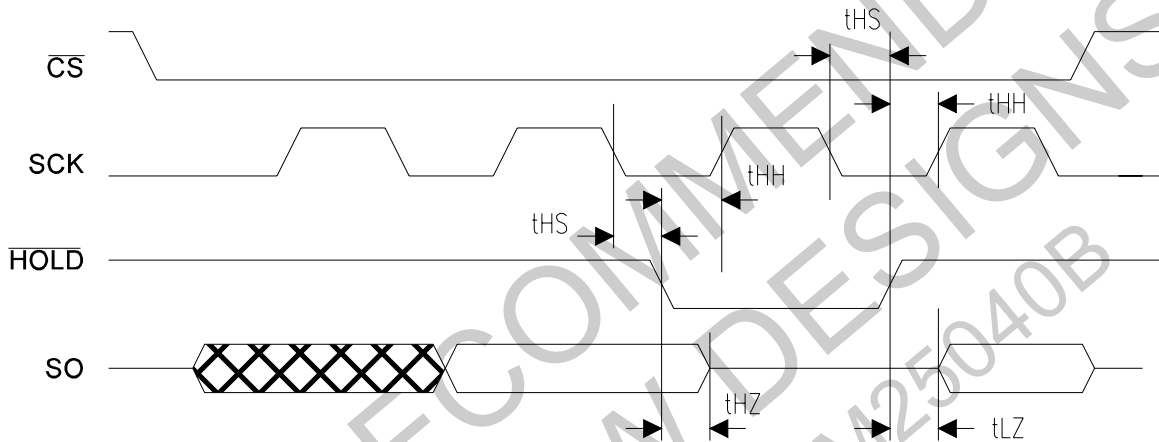
**AC Test Conditions**

Input Pulse Levels	10% and 90% of $V_{DD}$
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	$0.5 V_{DD}$
Output Load Capacitance	30 pF

Serial Data Bus Timing



/Hold Timing

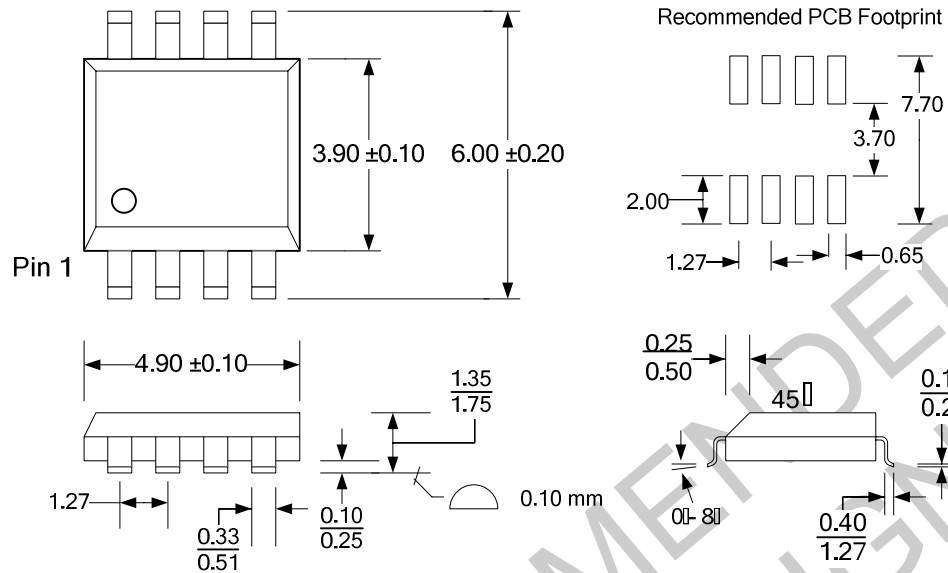


Data Retention ( $V_{DD} = 4.5V$  to  $5.5V$ ,  $+85^\circ$ )

Parameter	Min	Units	Notes
Data Retention	45	Years	

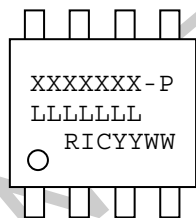
**Mechanical Drawing**

**(8-pin SOIC - JEDEC Standard MS-012, Variation AA)**



Refer to JEDEC MS-012 for complete dimensions and notes.  
All dimensions in millimeters.

**SOIC Package Marking Scheme**



**Legend:**

- XXXX= part number, P= package type
- LLLLLL= lot code
- RIC=Ramtron Int'l Corp, YY=year, WW=work week

Example: FM25040A, "Green" SOIC package, Year 2004, Work Week 50  
 FM25040A-G  
 A40003G1  
 RIC0450

**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Summary</b>
0.1	7/15/04	Initial Release
0.11	12/7/04	Added comment in Overview about differences between A and non-A devices. Rewrote chip select operation in Protocol Overview section (pg. 3). Updated mechanical drawing with pcb footprint.
2.0	4/11/05	Changed to Pre-Production status. Changed Data Retention spec. Added ESD and package MSL ratings.
3.0	5/5/06	Changed to Production status.
3.1	5/26/2009	Added tape and reel ordering information. Added last time buy notice on -S ordering numbers.
3.2	2/18/2011	Not recommended for new designs. Alternative: FM25040B.

NOT RECOMMENDED  
FOR NEW DESIGNS  
Alternative: FM25040B